In the claims:

1-11 (canceled)

12. (currently amended) A semiconductor device manufactured using the following process:

providing a semiconductor device having at least one metal interconnect layer completed;

then applying a planarizing dielectric layer on top of the semiconductor device and the metal interconnect layer; and

then providing a hydrogen treatment until hydrogen diffuses throughout and substantially saturates the semiconductor device.

13. (previously presented) The semiconductor device of Claim 12, wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen rich environment.

14. (previously presented) The semiconductor device of Claim 12, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

15. (previously presented) The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

16. (previously presented) The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

17. (previously presented) The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

18. (previously presented) The semiconductor device of Claim 12, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layers of dielectric material.

19. (previously presented) The semiconductor device of Claim 12, wherein the semiconductor device undergoes an N_2 bake after an HSQ of a multilayer planarizing dielectric layer is added.

20. (previously presented) The semiconductor device of Claim 12, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.

21. (currently amended) A semiconductor device manufactured using the following process:

providing a semiconductor device having thereon at least one metal interconnect layer completed; and

then providing a hydrogen treatment until hydrogen diffuses throughout and substantially saturates the semiconductor device.

22. (previously presented) The semiconductor device of Claim 21 wherein the hydrogen treatment includes heating the semiconductor device in a hydrogen environment.

23. (previously presented) The semiconductor device of Claim 21, wherein the hydrogen treatment includes applying hydrogen in situ by introducing hydrogen as a plasma to the semiconductor device.

24. (currently amended) The semiconductor device of Claim 21, further including a planarizing dielectric on said semiconductor device and said metal interconnect layer wherein the planarizing dielectric layer includes a first layer of TEOS, a second layer of HSQ, and a third layer of TEOS.

25. (currently amended) The semiconductor device of Claim 21, further including a planarizing dielectric on said semiconductor device and said metal interconnect layer wherein the planarizing dielectric layer includes a first layer of TEOS applied by PECVD.

26. (currently amended) The semiconductor device of Claim 21, further including a planarizing dielectric on said semiconductor device and said metal interconnect layer wherein the planarizing dielectric layer includes a second layer of HSQ applied by coating applied over a first layer of dielectric material.

27. (previously presented) The semiconductor device of Claim 21, wherein the planarizing dielectric layer includes a third layer of TEOS applied by PECVD applied over two layers of dielectric material.

28. (previously presented) The semiconductor device of Claim 21, wherein the semiconductor device undergoes an N_2 bake after an HSQ of a multilayer planarizing dielectric layer is added.

29. (previously presented) The semiconductor device of Claim 21, wherein the semiconductor device undergoes the hydrogen treatment after a final layer of the planarizing dielectric layer is added.